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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	8

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/712,173	LEE, TERRY R.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment A filed December 12, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-86 and 88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-69,72-86 and 88* is/are rejected.

7)☒ Claim(s) *70 and 71* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to Amendment A filed December 12, 2003.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4, 5, 7, 8, 13, 14, 44, and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4, 5, 7, and 8 recite the limitation "said first and second conductors". There is insufficient antecedent basis for this limitation in the claim.

Claims 13 and 14 recite the limitation "said plurality of regenerated data write clock signals".

Claims 44 and 45 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relationships between "said circuitry" and properties of the clock signal paths.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 6-11, 21-24, 33 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Perino et al., U.S. Patent No. 6,426,984 ("Perino").

As per claim 1, Perino discloses a method of providing clocking signals over a bus, said method comprising:

providing a first clock signal which travels over a first conductive path of said bus in a first direction (Fig. 5, clock1 over paths 28 and 32);

providing a second clock signal which travels over a second conductive path of said bus in a second direction opposite to said first direction (clock2 over paths 30 and 34); and

causing said first and second clock signals to have a predetermined phase relationship with respect to each other at a predetermined location on said bus (circuit 74 adjusts clock latency at nodes A and B).

As per claim 2, Perino discloses said predetermined phase relationship is substantially an in-phase relationship (Col. 6, lines 32-38).

As per claim 3, Perino discloses said detecting the phase relationship of said first and second clock signals at said predetermined location and adjusting at least one of said first and second clock signals (Fig. 5).

As per claim 6, Perino discloses data write clock and data read clock signals (Fig. 5).

As per claims 7 and 8, Perino discloses said predetermined location is along the length of said first and second conductive paths.

As per claim 9, Perino discloses each of said input/output devices comprise a memory subsystem (Claim 20).

As per claims 10 and 11, Perino discloses the phase deviations of said data write and data read clock signals (Col. 5, lines 50-60).

As per claim 21, Perino discloses at least one memory subsystem (Claim 20) and obtaining said predetermined phase relationship at said predetermined location (Col. 6, lines 32-38).

As per claim 22, Perino discloses said data write signal path is terminated (Fig. 5, termination block 31)

As per claims 23 and 24, Perino discloses said data read clock signal path is a loop back signal path (path 28).

As per claim 33 and 34, Perino discloses minimizing the phase between the data read clock and data write clock signals (Col. 5, lines 50-60).

4. Claims 84 and 85 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamagishi et al., U.S. Patent No. 6,366,190 ("Yamagishi")

As per claim 84, Yamagishi discloses a memory module (Fig. 1, storage apparatus) comprising:

a plurality of memory devices provided on a support structure (storage elements 5a-n);

a plurality of data read clock lines for receiving and providing respective data read clock signals to said plurality of memory devices (Col. 3, lines 56-60, for clocking read signals);

a data write clock line for receiving a data write clock signal (basic clock); and

a data write clock regeneration circuit coupled to said write clock line and said memory devices for respectively providing a plurality of regenerated data write clock signals to said memory devices (clock generator 4).

As per claim 85, Yamagishi discloses a register for receiving at least one of command and address signals, the outputs of said register couple to said memory devices, said data write clock regeneration circuit providing a regenerated data write clock signal to said register (Fig. 4, group 22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, as applied to claim 9 above, in further view of Yamagishi et al., U.S. Patent No. 6,366,190 ("Yamagishi").

As per claims 12 and 29, Perino does not expressly teach details of the memory subsystem to include a date write clock regeneration circuit. Yamagishi teaches a data write clock regeneration circuit for providing a plurality of regenerated data write clock signals to memory storage devices (Fig. 1, clock generator 4 and storage elements 5a-n). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Yamagishi's

data write clock regeneration to Perino's method. A motivation for doing so would have been to ensure the integrity of the system by compensating for loading of the clock signal.

6. Claims 15-20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, as applied to claim 9 above, in further view of Magro et al., U.S. Patent No. 6,516,362 ("Magro").

As per claims 15-20, Perino does not expressly teach details of the method o include a data read clock regeneration circuit. Magro teaches a coupling a clock regeneration circuit coupled to a clock signal path (Fig. 2b, clock driver 116). At the time of the invention, it would have been obvious to one skilled in the art to apply Magro's clock regeneration circuit to Perino's read clock signal path. A motivation for doing so would have been to compensate for loading of the clock signal (Magro, Col. 11, lines 5-10). Since Magro teaches a plurality of signal paths (Fig. 2b, output from clock driver 116), Perino/Magro further teaches a plurality of additional read clock signal paths.

7. Claims 30-32, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Yamagishi, as applied to claim 29 above, in further view of Magro et al., U.S. Patent No. 6,516,362 ("Magro").

As per claims 30-32 and 35, Perino/Yamagishi does not expressly teach issuing a plurality of data read clock signals from said memory controller. Magro teaches a coupling a clock regeneration circuit coupled to a clock signal path (Fig. 2b, clock driver 116). At the time of the invention, it would have been obvious to one skilled in the art to apply Magro's clock regeneration circuit to Perino's read clock signal path. A motivation for doing so would have

been to compensate for loading of the clock signal (Magro, Col. 11, lines 5-10). Since Magro teaches a plurality of signal paths (Fig. 2b, output from clock driver 116), Perino/Magro further teaches a plurality of additional read clock signals.

As per claim 36, Yamagishi teaches registers for receiving data in general at the memory subsystem (Fig. 4, group 22). Magro teaches command and address data paths, separate from the read/write data paths, that lead to the memory subsystem (Fig. 2b). Thus it would have been obvious to a have a register for command and address data.

8. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Yamagishi/Magro, as applied to claim 36 above, in further view of Mizukami et al., U.S. Patent No. 5,422,858 ("Mizukami").

As per claim 37, Perino/Yamagishi/Magro does not expressly teach the data write signal provided to said register is at a lower frequency than the data write clock signals provided to said memory devices. Mizukami teaches multiplying clock signals provided to said memory devices (Fig. 3, multiplied clock provided to ram core). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Mizukami's clock multiplying to Perino/Yamagashi/Mago's method. A motivation for doing would have been to optimize clock timing within the memory devices (Yamakagashi, Col. 1, line 58 – Col. 2, line 5).

9. Claims 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, as applied to claim 9 above, in further view of Gillingham et al., U.S. Patent No. 6,510,503 ("Gillingham").

As per claim 38, Perino does not expressly teach a memory module capable of being connected to said bus. Gillingham teaches such a memory module (Figs. 14a &b). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gillingham's socket to Perino's method. A motivation for doing so would have been to facilitate replacement by modularizing components.

As per claim 39-41, Gillingham teaches each memory subsystem comprises a plurality of memory storage devices (Figs. 13 and 14).

10. Claims 25-28 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, as applied to claims 1, 3, 6, and 21 above, in further view Gasbarro et al., U.S. Patent No. 5,432,823 ("Gasbarro").

As per claim 42, Perino teaches a clock system for a data bus, comprising:

a data bus comprising:

a plurality of data paths (Col. 1, lines 14-18, 48-59);

a first clock signal path for propagating a first clock signal in a first direction along said bus (Fig. 5, paths 28 and 32 for clock1);

a second clock signal path for propagating a second clock signal in a second direction opposite to said first direction along said bus (paths 30 and 34 for clock2);

a bus controller for issuing second clock signal in said second clock signal path (master 24); and

circuitry for causing said first and second clock signals to have a predetermined phase relationship with respect to each other at a predetermined location along said bus (circuit 74).

Perino does not expressly teach issuing said first clock signal from said bus controller. Perino does teach changing the location of the circuitry (Figs. 5 & 8, circuit 74 is moved from clock generator 72 to master 24). Gasbarro teaches a bus controller that issues both clock signals (Fig. 2, master device). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gasbarro's issuing said first clock signal from the bus controller to Perino's clock system, since Gasbarro is incorporated by reference (Col. 1, lines 14-18).

As per claim 25, Gasbarro teaches terminating said loop back signal path at said memory controller (Fig. 2, RLCK0 and RCLK1).

As per claim 26, since the bus controller issues both data write clock and data read clock signals, it would have been obvious to derive both clocks from the same clock source in order to avoid the complexity of an additional clock generator.

As per claim 27, Perino teaches using a phase lock loop (Col. 6, lines 32-38).

As per claim 28, Perino teaches adjusting the relative phase relationship (Col. 6, lines 1-14).

11. Claims 68, 69, 72, 73 and 78-83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino et al., U.S. Patent No. 6,426,984 ("Perino"), in view Gasbarro et al., U.S. Patent No. 5,432,823 ("Gasbarro"), further in view of Gillingham et al., U.S. Patent No. 6,510,503 ("Gillingham").

As per claim 68, Perino teaches a memory system comprising:

a data bus comprising read/write data path (Fig. 1, data bus 36), a data write clock signal path for propagating a data write clock signal in a first direction along said bus (Fig. 5, paths 30 and 34 for clock2), and a data read clock signal path for propagating a data read clock signal in a second direction along said bus (paths 28 and 32 for clock1), said second direction being opposite said first direction;

a memory controller coupled to said bus (master 24; Claim 21) for respectively issuing said date write and data read clock signals on said data write and data read clock signal paths and for setting a predetermined phase relationship between said data write and data read clock signals at a predetermined phase relationship between said data write and data read clock signals at a predetermined location along said bus (Fig. 8, circuit 74 located in master 24); and

at least one memory subsystem couple to said bus for exchanging data with said memory controller in accordance with timing set by said data write and data read clock signals (slaves 26A-N; Claim 20).

However Perino does not expressly teach details of the data bus such as having a plurality of data paths. Gillingham teaches a plurality of data paths, of which a plurality are read/write data paths (Fig. 2a). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gillingham's read/write data paths to Perino's data bus. A motivation for doing so would have been to ensure the integrity of the memory system for transferring data.

Perino also does not expressly teach issuing said first clock signal from said bus controller. Perino does teach changing the location of the circuitry (Figs. 5 & 8, circuit 74 is moved from clock generator 72 to master 24). Gasbarro teaches a bus controller that issues both

clock signals (Fig. 2, master device). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gasbarro's issuing both clock signals from the bus controller to Perino's memory system, since Gasbarro is incorporated by reference (Col. 1, lines 14-18).

As per claim 69, Gillingham teaches a memory subsystem comprising a plurality of memory devices (Fig. 14a, memory devices 196).

As per claim 72, Perino teaches an associated phase lock loop for maintaining said predetermined phase relationship (Fig. 6).

As per claim 78, Perino teaches said data write signal path is terminated (Fig. 5, termination block 31), and said data read clock signal path is a loop back signal path (path 28).

As per claims 79 and 80, Gasbarro teaches terminating said loop back signal path at said memory controller (Fig. 2, RLCK0 and RCLK1).

As per claims 73, 81 and 82, Perino teaches a plurality of memory subsystems (Fig. 5, slaves 26A-N) and minimizing clock latency (Col. 5, lines 50-60).

As per claim 83, since Perino/Gasbarro/Gillingham teaches teaches the memory system of claims 68, 69, 72, 73 and 78-83, the combination teaches the claimed memory system.

12. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Gasbarro/Gillingham, as applied to claim 68 above, in further view of Yamagishi et al., U.S. Patent No. 6,366,190 ("Yamagishi").

As per claim 74, Perino/Gasbarro/Gillingham, as applied to claim 68, does not expressly teach details of the memory subsystem to include a date write clock regeneration circuit.

Yamagishi teaches a data write clock regeneration circuit for providing a plurality of regenerated data write clock signals to memory storage devices (Fig. 1, clock generator 4 and storage elements 5a-n). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Yamagishi's data write clock regeneration to Perino/Gasbarro/Gillingham's memory subsystem. A motivation for doing so would have been to ensure the integrity of the system by compensating for loading of the clock signal.

13. Claims 43-67, and 75-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Gasbarro/Gillingham, as applied to claims 42 and 68 above, in further view of Magro et al., U.S. Patent No. 6,516,362 ("Magro").

As per claim 75, Perino/Gasbarro/Gillingham, as applied to claim 68, does not expressly teach details of the memory system to include a data read clock regeneration circuit. Magro teaches a coupling a clock regeneration circuit coupled to a clock signal path (Fig. 2b, clock driver 116). At the time of the invention, it would have been obvious to one skilled in the art to apply Magro's clock regeneration circuit to Perino/Gasbarro/Gillingham's read clock signal path. A motivation for doing so would have been to compensate for loading of the clock signal (Magro, Col. 11, lines 5-10). Since Magro teaches a plurality of signal paths (Fig. 2b, output from clock driver 116), Gasbarro/Magro further teaches a plurality of additional read clock signal paths.

As per claim 76, Gillingham teaches a motherboard (Fig. 13a).

As per claim 77, Gasbarro teaches a transmitting device which generates data write clock and read clock signals (Fig. 3, element 132).

As per claims 43-67, since Perino/Gasbarro/Gillingham/Magro teaches the memory system of claims 68, 69, 72, 73 and 75-82, the combination teaches the claimed clock system.

14. Claim 86 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al., U.S. Patent No. 6,366,190 ("Yamagishi"), as applied to claim 84 and 85 above, in further view of Mizukami et al., U.S. Patent No. 5,422,858 ("Mizukami").

As per claim 86, Yamagishi does not expressly teach the data write signal provided to said register is at a lower frequency than the data write clock signals provided to said memory devices. Mizukami teaches multiplying clock signals provided to said memory devices (Fig. 3, multiplied clock provided to ram core). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Mizukami's clock multiplying to Yamagashi's memory module. A motivation for doing would have been to optimize clock timing within the memory devices (Yamakagashi, Col. 1, line 58 – Col. 2, line 5).

15. Claim 88 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gasbarro et al., U.S. Patent No. 5,432,823 ("Gasbarro"), in view of Magro et al., U.S. Patent No. 6,516,362 ("Magro").

As per claim 88, Gasbarro teaches a bus structure for memory system comprising:

a plurality of data paths (Fig. 3, data bus 120);

a first write clock signal path for propagating a data write clock signal in a first direction along said bus (Fig. 2, TCLK path); and

a second read clock signal path for propagating a data read clock signal along said bus (RCLK path).

However, Gasbarro does not expressly teach a data read clock regneration circuit coupled to said second read clock signal. Magro teaches a coupling a clock regeneration circuit coupled to a clock signal path (Fig. 2b, clock driver 116). At the time of the invention, it would have been obvious to one skilled in the art to apply Magro's clock regeneration circuit to Gasbarro's read clock signal path. A motivation for doing so would have been to compensate for loading of the clock signal (Magro, Col. 11, lines 5-10). Since Magro teaches a plurality of signal paths (Fig. 2b, output from clock driver 116), Gasbarro/Magro further teaches a plurality of additional read clock signal paths.

Allowable Subject Matter

16. Claims 70 and 71 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
March 5, 2004

Dennis M. Butler

Dennis M. Butler
Primary Examiner